Test and Reliability of Integrated Circuits and Systems

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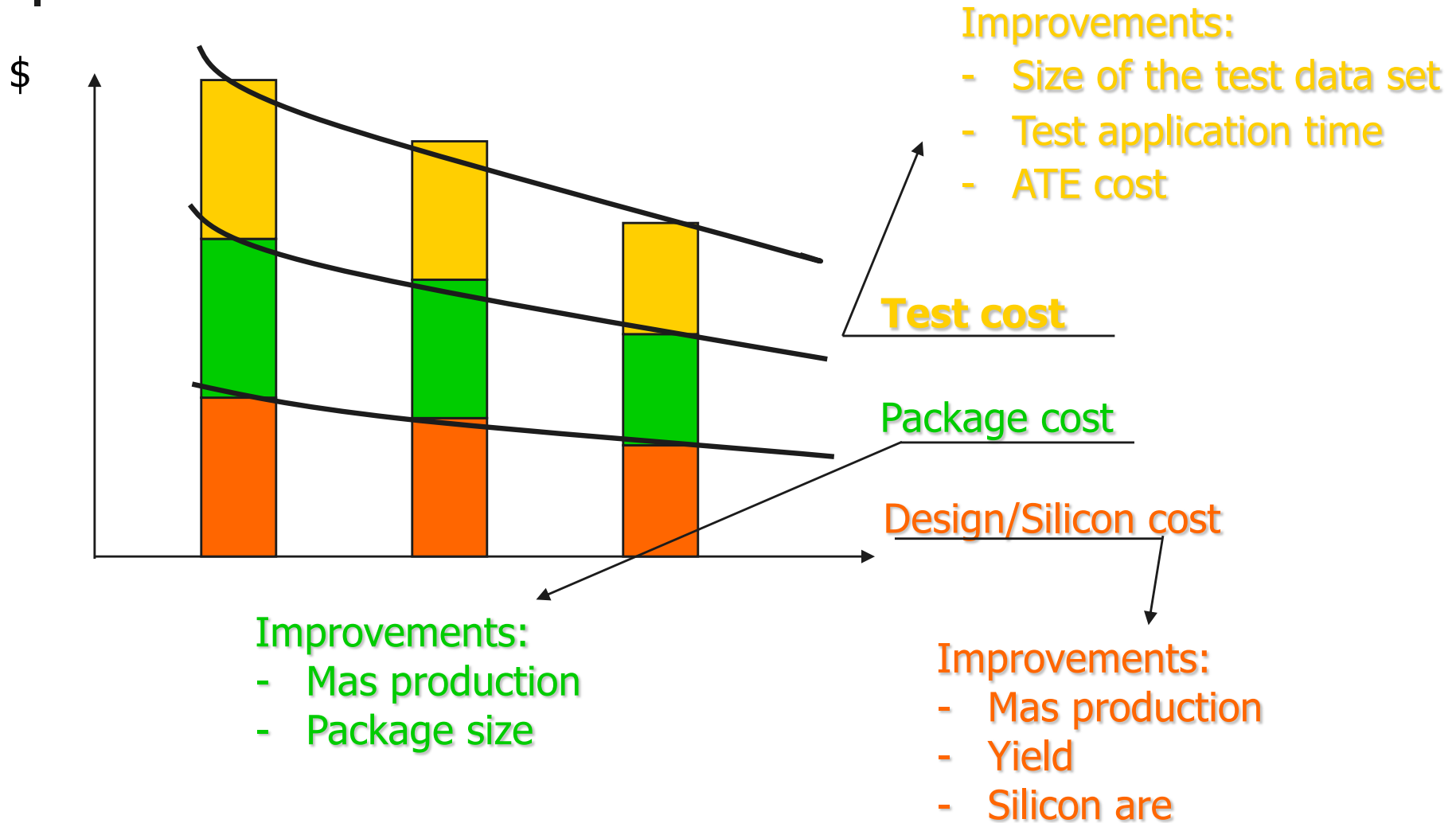# Chapter 1
Introduction

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Verification versus Test

- To verify the correctness of the design
- Done by simulation, hardware emulation, formal proof
- Performed before fabrication steps
- Responsible of the design quality

- To verify the correctness of the manufactured device
- Done in tow steps:
  - Test program generation: performed during the design phase
  - Test application: electrical tests applied after manufacturing
- Electrical tests are:
  - Applied on each manufactured devices
  - Responsible of the device quality
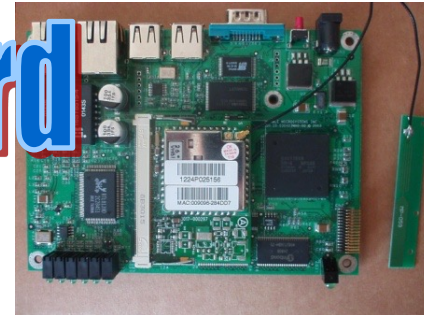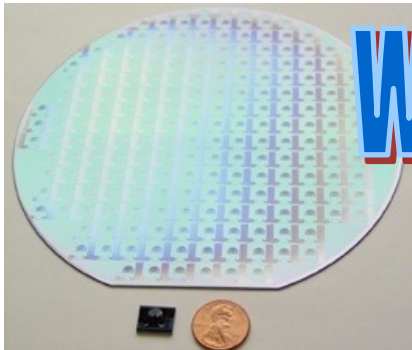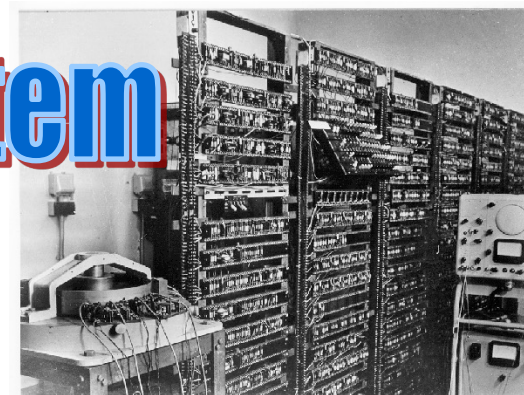
ICs Production Cost

$

Improvements:
- Size of the test data set
- Test application time
- ATE cost

Test cost

Package cost

Design/Silicon cost

Improvements:
- Mas production
- Package size

Improvements:
- Mas production
- Yield
- Silicon are

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When Test?

Circuit

Board

Wafer

System

When Test?

DUT – Device Under Test			
Wafer	**Package**	**Board**	**System**
Test of the technological process	Parametric test	"Entrance" test	System test
Test of dies	Logic test	Board test	In-use test
	Aging (burning test)	Finalized board test	
	Full test on samples	Aging	

Test Results

Reality

Results

TEST:
ATE,
sequence,
parameters

OK

$\overline{\text{OK}}$

$\overline{\text{OK}}$

OK
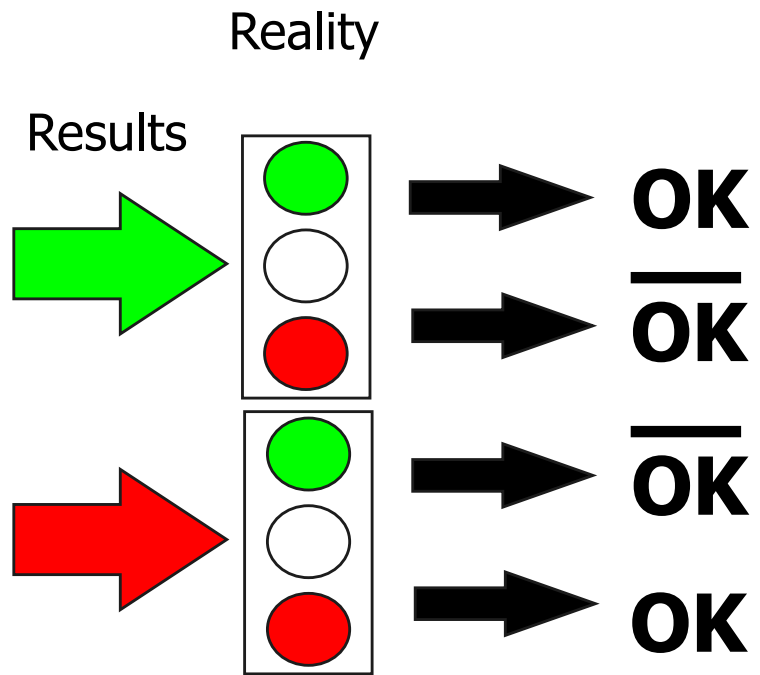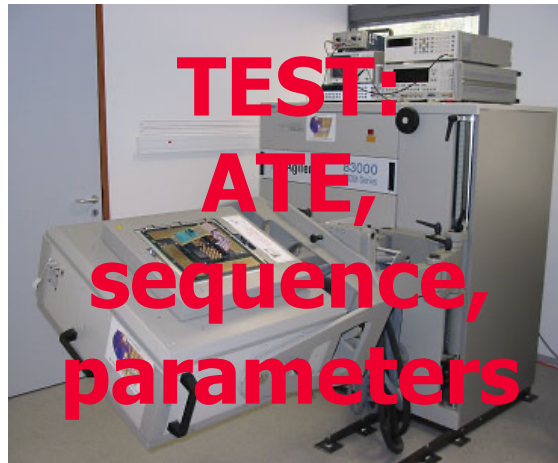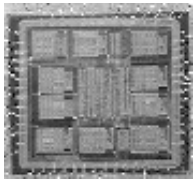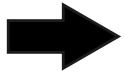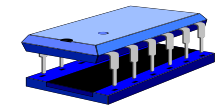
ATE – Expensive equipment (M$)

Some Definitions and Terminologies (1)

- Testing is possible when one can apply a known stimulus to an entity in a known state and when the known response can be evaluated

  - **known stimulus:** access to the DUT inputs and apply a known value
  ⇒ CONTROLABILITY

  - **Known response:** access to the DUT outputs and comparison with the golden one
  ⇒ OBSERVABILITY

Some Definitions and Terminologies (2)

- **Error:** erroneous observed behavior
- **Fault:** deviation of the structure from the specifications
- **Defect:** deviation of the physical realization from the manufacturing specifications
- **Failure:** malfunction in operation
- **Test:** fault detection
- **Diagnosis:** fault localization